The Effect of Device Scaling on Single-Event Effects in Advance CMOS Devices

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I. INTRODUCTION

Single-event upset of microelectronics in space was first reported by Binder, Smith and Holman in 1975 [1]. Improvements in semiconductor device design and performance in the ensuing 29 years have resulted in mainstream devices with feature size below 0.1 µm, and more than 10^8 transistors per chip. No one could have predicted such a dramatic evolution in this field. Along with these increases in density and performance, there has been increasing concern about single-event upset in terrestrial applications from alpha particles and neutrons).

The first efforts to predict how device scaling would impact single-event upset in space were done by Petersen, *et al.* in 1982 [2]. Figure 1, adapted from that work, has been widely used, and has turned out to be a surprisingly good predictor of critical charge over several generations of devices.
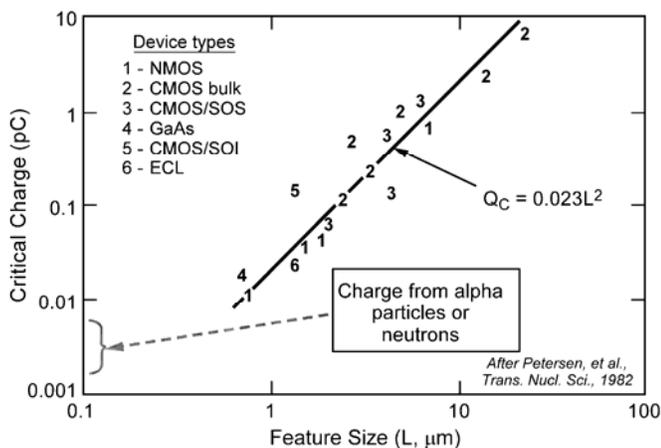

Fig. 1. Critical charge vs. feature size (after Petersen, *et al.* [2].) The figure has been revised to show the expected "plateau" from concern about alpha particles and atmospheric neutron effects.

Initially the issues for space applications were overcome by designing special hardened circuits. For example, adding resistors to SRAMs slows down the response, improving the SEU hardness by large factors [3] (*however, that approach is impractical for modern high-speed SRAMs*). Although a limited number of hardened circuits are available, the performance of hardened devices lags commercial technology by at least two generations, restricting the performance of hardened technologies for spacecraft designers. Consequently there is considerable interest in using state-of-the-art commercial integrated circuits in space,

even though spurious responses due to SEU effects have to be taken into account in overall system design when unhardened devices are used.

Single-event upset from alpha particles that are produced from radioactive decay became an issue for commercial semiconductor manufacturers in 1979 [4]. As devices have been scaled to even smaller feature sizes, the semiconductor industry has also been forced to deal with upset from neutrons, produced by the interaction of cosmic rays in the upper atmosphere, that are present in significant numbers at the earth's surface. Most manufacturers analyze and test their products to verify acceptable soft error rates, and this has been used to modify the critical charge relationship of Petersen, *et al.* in the dashed line of Figure 1.

Neutrons and protons with energies above 30 MeV cause very similar reactions with silicon. Thus, the concern – and moderate hardening of commercial semiconductors to atmospheric neutrons – is directly applicable to upset from energetic protons in space. However, upset from highly energetic cosmic rays is not considered by the commercial semiconductor industry. The charge deposited by cosmic rays is considerably higher than charge produced by either alpha particles or neutrons, and thus nearly all unhardened high-density integrated circuits are susceptible to upset from heavy ions in space.

This paper discusses the effects of device scaling on upset sensitivity for commercial CMOS circuits in space applications. This topic is extremely important for NASA space applications because significant numbers of unhardened commercial microelectronic devices are used in nearly all NASA spacecraft. Examples of critical components include dynamic random access memories (DRAMs), used in solid-state recorders; flash memories; field-programmable gate arrays; and high-performance microprocessors.

The next section of the paper discusses scaling concepts, based on design requirements for various circuit applications, along with predicted improvements and process changes from the Semiconductor Industry roadmap [5]. The third section discusses charge generation and collection, along with basic mechanisms for producing upsets in highly scaled devices. Section IV discusses recent experimental results for state-of-the-art commercial CMOS, benchmarking these results for devices with feature sizes between 0.13 and 0.35 µm. The last section puts these results into perspective, and makes predictions about the way in which future

changes in technology and scaling are likely to affect single-event susceptibility in space.

Although total dose damage is potentially an issue for some space applications, charge trapping is so small in the thin gate oxides used in highly scaled devices that gate threshold shifts are no longer of much concern except for circuits with high internal voltages (such as flash memories). Total dose effects in the compact trench isolation structures used for highly scaled circuits are potentially important, but tests of advanced microprocessors have shown negligible degradation at levels below 100 krad(Si). For these reasons, total dose effects have not been included in this paper, although they continue to be important for some technologies, such as DRAMs.

II. SCALING RELATIONSHIPS

A. General Issues for Conventional CMOS

Device scaling for CMOS is a complex problem, which requires tradeoff of many different parameters [6-8]. Initial scaling predictions were done with constant voltage, introducing the concept of scaling factors for device dimensions (including channel length and gate oxide thickness) but requiring scaled devices to function with 5-V power supplies.

Later work allowed reduced power supply voltage, using the concept of constant field scaling where the electric field in the channel region is held constant [9]. Doping levels, channel length and oxide thickness are allowed to change with the scaling factor. Constant-field scaling assumes that all key device parameters are scalable. It is oversimplified for power supply voltage (V_{DD}) below two volts because threshold voltage and subthreshold slope, which do not scale, become a significant fraction of V_{DD}.

A different approach was developed in the last ten years where the electric field in the channel region and the field across the gate oxide are allowed to *increase* [6]. The increased fields are essential in order to get sufficient improvement in device performance. Fig. 2, after Davari, *et al.*, shows predictions of the channel electric field and power supply voltage for two different scaling scenarios [6]. Although those predictions were made in 1995, they are close to the values used for current production circuits.

Analysis of scaling effects is quite complex. Many older scaling projections have overestimated reductions in power supply voltage and threshold voltage for channel lengths below 100 nm. The latest scaling predictions use a modification of this concept, providing separate dimensional scaling parameters for channel length and a less aggressive scaling factor for channel width and wiring [8].
Scaling also depends on circuit applications. Recent work has subdivided scaling into three basic circuit applications: (1) high-performance devices, such as microprocessors, where the main overall criterion is speed; (2) low-power devices, where speed and power dissipation are both involved in establishing design tradeoffs; and (3) memories,

which require a different set of tradeoffs. One critical parameter is the "on/off" ratio, the current ratio between a device that is driven into saturation, and one that is switched off. The subthreshold slope (85 to 100 mV per decade of current for typical devices) places a fundamental limit on the on/off ratio. Details associated with the various scaling scenarios are discussed below.
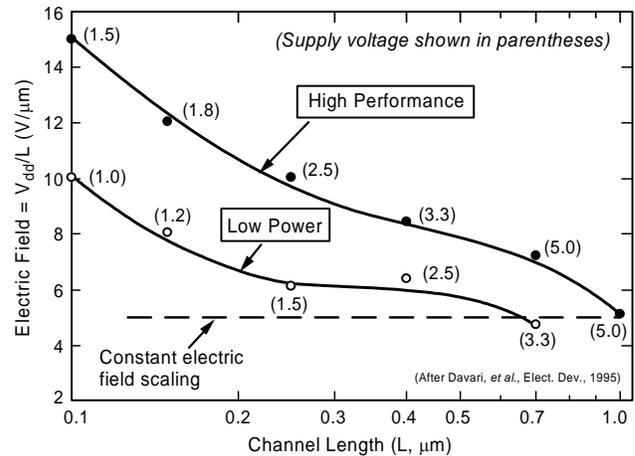

Fig. 2. Channel electric field and power supply voltage scaling predictions.

High Performance Devices. For high-performance devices, power dissipation is a key issue, but the design criteria allow design of circuits that can dissipate large amounts of power (i.e., the fan-cooled packages in high-speed microprocessors). Because the device normally operates at high frequency, standby current and gate leakage currents can be much higher than for other scaling scenarios.

Recent versions of the Semiconductor Road map include several different subcategories for high-performance scaling. The most aggressive is intended for server applications that dissipate extremely high amounts of power. This category is inconsistent with space applications, where more realistic limits need to be placed on power requirements. Therefore the appropriate scaling path for high-performance devices in space roughly follows scaling for devices used in desktop computers, which is less aggressive than applications in servers where very high power dissipation can be tolerated. The "on/off" current ratio is considerably higher for that scaling scenario compared to the more extreme limits for server applications, requiring higher power supply voltage as well as thicker gate oxides.

Gate leakage has become a major issue for scaled devices because of tunneling through very thin oxides. Current projections for high-performance devices are based on assigning 10 to 20% of the total power to gate leakage, which is a major departure from earlier scaling assumptions. Note that gate leakage does not scale with frequency, so that a significant fraction of the total power is effectively standby power when this tradeoff is made. Again, somewhat thicker gate oxides are required for the more moderate high performance category.

Low Power. Low power devices place more stringent demands on standby power, and may also implement a reduced voltage mode to further reduce power during periods when maximum performance is not required. One of the main differences is the requirement for thicker gate oxides compared to high-performance devices in order to reduce gate leakage effects. Initial scaling projections for low-power applications used much lower power supply voltage compared to high-performance scaling, but more recent scaling projections use nearly the same voltages for both scenarios. The reason for this is the need for high on/off ratios for low-power applications.

Memories. Memories involve very different tradeoffs compared to speed-driven technologies, such as microprocessors. The on/off current ratio for memories needs to be about two orders of magnitude higher for memories than for logic. This requires thicker gate oxides compared to logic applications. Changes in device architecture and (for DRAMs) the design of the storage capacitor are key factors in memory evolution. An older prediction of memory trends is shown in Fig.3, after Itoh [11]. Although the cell area decreases sharply with scaling, the total charge on the storage capacitor is reduced only slightly. This is required in order to maintain an acceptable retention time. Another important constraint is that the charge stored on the capacitor remain above the charge produced by 5-MeV alpha particles in order to keep the soft error rate within acceptable limits.
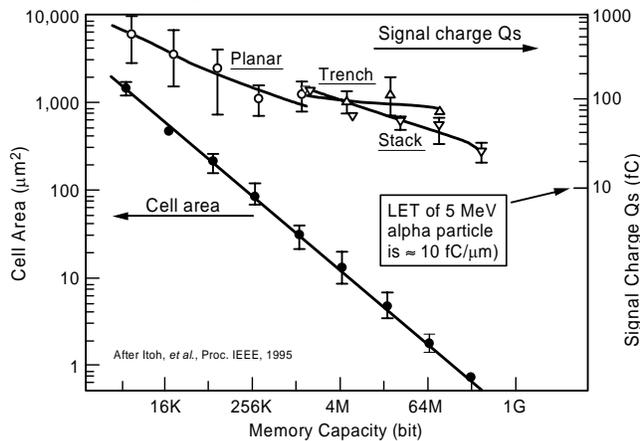

Fig. 3. Scaling predictions for DRAM technology.

Trench capacitors with very high aspect ratios have been developed during the last five years to minimize cell area. As discussed later, capacitor design has a large impact on single-event upset sensitivity.

Leakage currents in DRAMs must be very low in order to meet refresh rate requirements. Variations in threshold voltage occur within a large DRAM for several reasons, including statistical fluctuations in the number of dopant atoms that are present in each device [11]. The threshold voltage variations cause large differences in leakage current, requiring considerably lower mean leakage currents in the

DRAM array in order to keep leakage currents in the more extreme part of the distribution within tolerance. Measurements of refresh rates over the entire DRAM array provide direct evidence of this effect [12].

Mainstream commercial memories are also extremely cost sensitive. Consequently, they use more conservative design approaches, and are nearly always made with bulk rather than epitaxial substrates. This makes them more susceptible to latchup than most logic-based circuits. Some advanced DRAMs are susceptible to catastrophic latchup from heavy ions. The bulk substrates allow charge collection from the extended region of the substrate when a device is struck with a heavy ion, increasing the likelihood of multiple-bit upsets compared to devices that are made on epitaxial substrates.

B. Silicon-on-Insulator

Silicon-on-insulator CMOS has many potential advantages. Much has been made of the potential advantage of the very shallow silicon film thickness - typically 120 – 200 nm for partially depleted SOI. In principle this should result in far less charge collection compared to bulk/epitaxial processes where the charge collection depth is approximately 2000 nm, resulting in much lower soft error rates as well as improved SEU hardness in space for SOI. However, in partially depleted structures excess charge collection can occur because of the parasitic bipolar transistor (unless body ties are used in the process), largely negating the advantage of the reduced charge collection region [13]. This will be discussed further in Section IV.

C. The Semiconductor Roadmap

The semiconductor industry has established a "roadmap" in order to facilitate overall planning for equipment manufacturers. The roadmap is updated periodically. Table 1 shows some key properties of predictions for high-performance devices, based on the 2002 SIA Roadmap [5]. Several things should be noted. First, there is a steady decrease in power supply voltage, which is required in order to keep power dissipation within reasonable bounds. This means that internal switching voltages for high-performance logic must continue to decrease, affecting noise margin as well as the allowable number of gates through which high-speed pulses can propagate (each transition reduces the

Table 1
Key Properties for High-Performance Devices

Year	2000	2001	2002	2003	2004	2005	2008	2011
T_{ox} (nm)	2.5	1.9	1.9	1.9	1.5	1.5	1.2	0.8
V_{dd} (V)	1.8	1.5	1.5	1.5	1.2	1.2	0.9	0.6
Gate Length (nm)	120	100	85	80	70	65	45	32
On/Off Ratio	107	94	75	58	47	38	19	9.4

switching amplitude somewhat, and eventually the pulses will no longer propagate). Second, the on/off ratio is rapidly decreasing, and actually changes more than any of the other parameters. It is predicted to decrease by a factor of ten during the current decade. Although this decrease can be tolerated in high-performance devices, it is clearly at odds with the requirements for low-power devices and memories. More realistic scaling scenarios require higher on-off ratios.

D. Device Design Anticipated for the Near Future

Older scaling scenarios assumed that the basic design of the fundamental CMOS structure changed very little as dimensions were reduced. However, modern MOS devices incorporate many design changes in order to achieve better performance. Figure 4 shows a physical diagram of an advanced CMOS device. Particular features include the use of special "halo" implants under the source and drain region to reduce the "rolloff" of threshold voltage for short channel lengths, and the use of complex retrograde doping profiles in the channel region. In highly scaled devices the doping profile is adjusted in both the lateral and transverse directions in order to confine carriers to the active region beneath the gate. Note also the extended transition region between the highly doped substrate and the epitaxial layer. Ions that strike that region contribute charge to the n-channel device, and the design of the substrate is a key factor in SEU sensitivity.
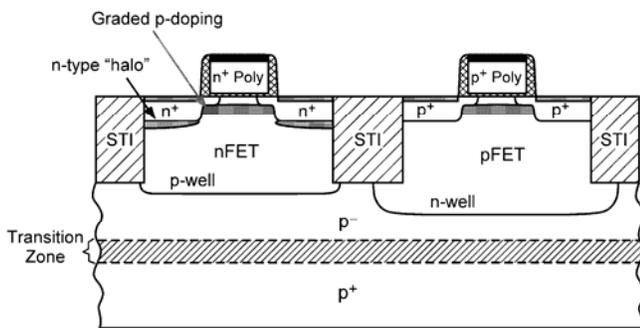
Fig. 4. Physical diagram of an advanced twin-well CMOS device on an epitaxial substrate.

Recent work by Frank, *et al*. projected an improved transistor that is intended for mainstream digital applications in the year 2008 [8]. That device is intended for 25 nm channel lengths, with a gate oxide thickness of 1.5 nm. The power supply voltage is 1 V, somewhat higher than that predicted by the semiconductor roadmap. Figure 5, from that work, shows the subthreshold characteristics of transistors with various channel lengths, showing excellent performance down to 20 nm. Note that the on-to-off current ration is nearly 10^4, considerably higher than the value assumed in the semiconductor roadmap. Fabrication details include use of very sharp doping profiles in the lateral and transverse directions of the channel region. This structure is probably more representative of mainstream digital device technologies than predictions from the SIA roadmap.
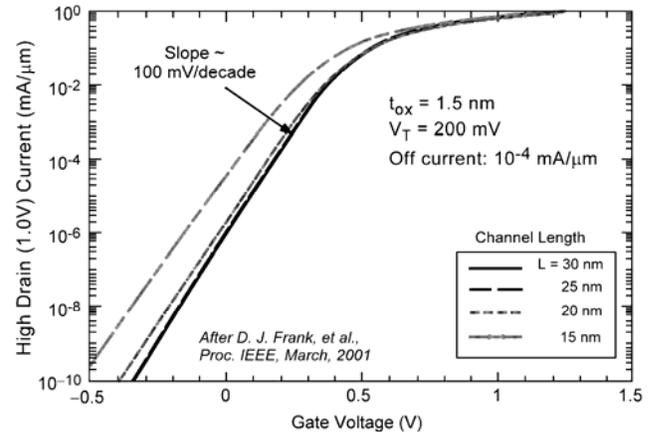
Fig. 5. I-V characteristics of an advanced CMOS device with channel lengths of 25 nm [9].

Doping profiles in the channel, drain and source of this device are shown in Fig. 6, along with equipotential contours [9]. Very abrupt changes in doping concentration are required in order to constrain the fields and carrier concentrations within the small dimensional limits of this device. The total area of a narrow width transistor fabricated with this process is approximately 0.01 μm^2.
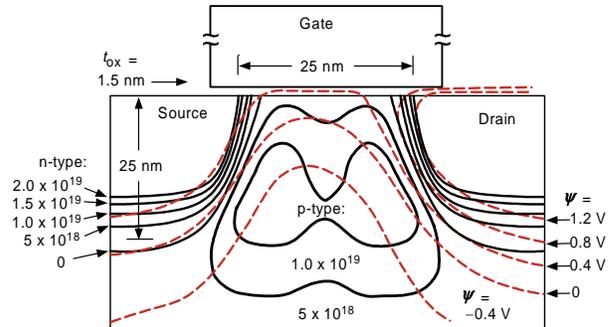
Fig. 6. Doping profile of an advanced NMOS transistor with gate length of 25 nm.

III. THE UPSET PROCESS

A. Charge Generation

Charge generated from a heavy ion is usually assumed to be proportional to linear energy transfer (LET), and to effectively create a dense line of charge within the structure. This concept has worked well for older devices, and continues to be a reasonable approach for alpha particles, which have relatively small track diameters (≈ 0.1 μm). A great deal of the charge generation work done in the device community has been done using the track diameter and charge density of 5-MeV alpha particles.

Particles in space have a broader charge-deposition structure because they have such high energies. Several studies have been done to calculate the track structure. Figure 7 (after Dodd, *et al*. [14]) shows how the track diameter of a 1-GeV silver ion changes as it traverses a silicon region. The incident LET of the ion is 46 MeV-cm^2/mg, with a range of about 70 μm. The track density is very high within the central core region, with an approximate

diameter of 0.1 μm. The track diameter extends to several microns for lower charge densities. That is not the case for ions with lower energy. The track of a 100-MeV silver atom has the same incident LET as that of the 1-GeV silver atom shown in the figure, but extends less than 1/100 as much as the track of the higher energy ion at the surface for lower charge densities.
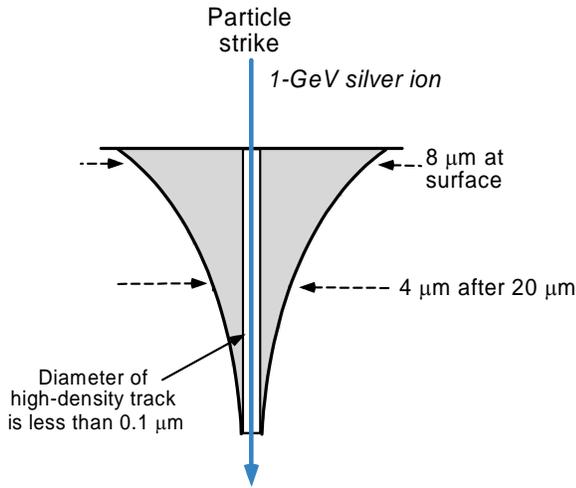

Fig. 7. Track structure of a 1-GeV silver atom. The carrier density in the central core exceeds 10^{21} carriers/cm^3. The carrier density in the lightly shaded region corresponds to about 10^{15} carriers/cm^3.

Near the threshold LET, the track structure is less important because the device response is dominated by charge in the central core. However, for particles with LET well above the threshold region the track structure of the ion extends over many different active devices (if the process has a small feature size), but produces less localized charge density within a single device than one would expect using LET as a figure of merit. The charge of a real particle in space is spread over a relatively broad region. The difference in track structure between ions available in the laboratory and the extremely energetic ions in space has to be taken into account in the interpretation of laboratory test results for scaled devices.

B. Charge Collection

Initial work on charge collection was done for structures with much larger areas than the highly scaled devices that are available today. Initial work by Hsieh, *et al.* showed that the collapse of the charge track along the path of an alpha particle allowed direct collection of prompt charge in a p-n junction at distances well beyond the depletion region (charge funneling [15]). The concept of funneling was further discussed by McLean and Oldham in 1992 and corroborated with charge-collection measurements on p-n junctions [16]. Since then, device analysis codes have been used to do more detailed studies of charge collection at time scales that provide better insight into charge funneling and device size effects. Funneling is less important for devices with thin epitaxial substrates, because the highly doped

substrate cuts off the charge collection. However, it continues to be important for highly scaled devices that are fabricated on lightly doped substrates, particularly for memories.

An example of how charge collection is affected by scaling is shown in Fig. 8, after Shin [17]. A 3-D modeling code was used to show how charge collected from an alpha particle strike was affected by the location of the ion strike within the structure, as well as the power supply voltage and the total junction area.
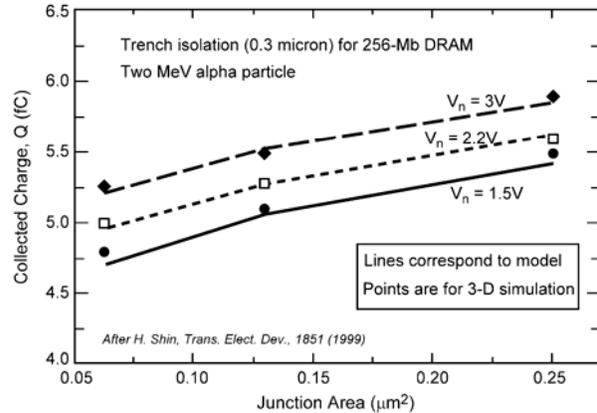

Fig. 8. Effect of ion strike position and power supply voltage on collected charge from a 2-MeV alpha particle strike [17].

These results show that the charge collected from the alpha particle strike is about 25% lower as junction area is reduced, along with slight reductions due to the decreased power supply voltage. The simulations correspond to particle strikes at the center of the drain region, where the structure is most sensitive to upset effects. They demonstrate one reason that upset sensitivity does not necessary increase for highly scaled devices. The effect of small device geometry on charge collection may be even larger for energetic ions in space which have a larger track radius compared to the alpha particle strikes that have been the focus of much of the work by semiconductor manufacturers.

More recent work on charge collection was done by Ferlet-Cavrois, *et al.*, as shown in Fig. 9 [18]. They calculated the charge collected in basic bulk and SOI transistors as the feature size and doping levels were changed in accordance with the SIA Roadmap using a 3-D computer modeling program. They predict a slight increase in total collected charge with decreasing feature size for bulk devices, and a much larger increase for SOI technology. As discussed later, these results do not agree with measurements on SOI processors with feature sizes as low as 0.13 μm that show nearly flat dependence of LET threshold, implying lower charge collection. They also conflict with results for bulk processors, which show slight decrease in SEU sensitivity for feature sizes between 0.4 and 0.18 μm.

Circuit design also influences single-event upset. Basic 6-T memory cells can be upset when the charge collected at the drain of the "off" transistor exceeds the critical charge

for upset. This critical charge depends on the switching margin (related to the threshold voltage and the voltage at which the circuit will actually switch); and total capacitance, which includes the capacitance from drain to substrate, gate capacitance, and stray capacitance in the isolation region. In the past, charge collected from the ion strike has been considered instantaneous, but newer device structures respond so quickly that the detailed time response of the charge collection process is also important. Estimates of critical charge can be determined with the SPICE program, but more precise calculations using 2-D or 3-D analysis codes are required for accurate analysis.
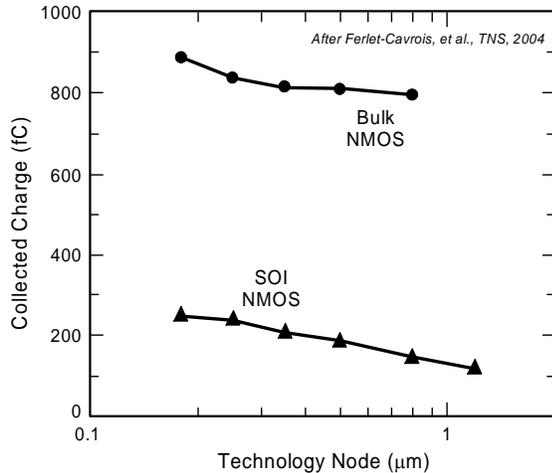

Fig. 9. Effect of scaling on charge collection predictions [18].

C. Circuit Effects

Critical charge is affected by design details, such as the channel width and loading, as well as differences in circuit implementation that involve multiple transistors in AND, NAND or NOR configurations. Domino CMOS and dynamic logic circuits are frequently used in high-performance devices, such as microprocessors. Those designs are far more complex than conventional clocked logic circuits, and it is not straightforward to evaluate the effects of internal transients on such designs.

Clock rates and switching chains can also affect critical charge; a chain of gates operating near the frequency limit will result in reduced logic swing as the switching pulse progresses through the chain [8]. This reduces the circuit margin, making the device more sensitive to single-event upset. Many papers have speculated that the narrowing "window" for upsets will make single-event upset effects far more severe as devices are scaled further. The narrow timing window and the reduced noise margin both influence frequency effects.

IV. RADIATION TEST RESULTS

A. DRAMs

Even though they are among the most sensitive devices to single-event upset, commercial DRAMs have been used during the last 15 years for solid-state recorder applications

on many spacecraft. Older DRAMs had very simple response modes, and it was possible to use elementary error-detection-and-correction algorithms in a straightforward way to correct upsets at the system level. For example, the Clementine spacecraft used an array of 4-Mb DRAMs in a 2.4-Gbit recorder, with a mean error rate of 71±2 errors per day [19]. Moon mapping with this storage approach was completely successful; no missing pixels occurred during the six months that the recorder was used.

Unfortunately newer DRAMs are not so easy to use in space because they are far more complex than earlier devices. Upsets in the internal architecture or control registers (for SDRAMs) can alter the functionality of the memory, creating large numbers of errors that cannot be dealt with in a straightforward manner. Multiple-bit upset from a single ion strike can also occur, with up to *several hundred* errors for ions with high LETs. However, if one ignores those complexities, the upset sensitivity of modern DRAMs on a per bit basis has actually improved as they have been scaled from the 16-Mb to the 256-Mb generation. Fig. 10 compares proton upset results for various devices, normalized to the error rate per bit. If the error rate were constant, then the cross section should decrease with the cell size. However, it is clear from this figure that there is a large change in the slope of this curve for more advanced DRAMs. The reason for this is changes in the way that the storage capacitor is designed in more advanced DRAMs. Trench capacitors with very large aspect ratios are used, reducing charge collected in the capacitor compared to earlier DRAM technologies.
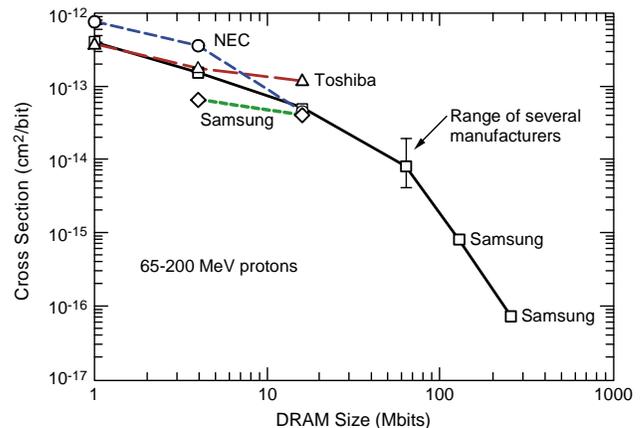

Fig. 10. Cross section for proton upset as DRAMs are scaled to smaller feature size.

Another important issue for advanced DRAMs is stuck bits. There are several possible mechanisms for stuck bits, but it is usually assumed that the mechanism is localized ionization damage (microdose) caused by the ion, which affects only a single device [20]. Microdose damage causes a shift in threshold voltage, increasing leakage current. For DRAMs the leakage current must remain very low in order to avoid refresh errors, particularly at moderately high

temperatures (50 – 70 °C) which is the typical operating temperature in DRAM arrays.

Figure 11 shows how the cross section for single-event upset and hard errors depends on linear energy transfer for a 64-Mb SDRAM. The ratio is only about 10,000 to 1, so the
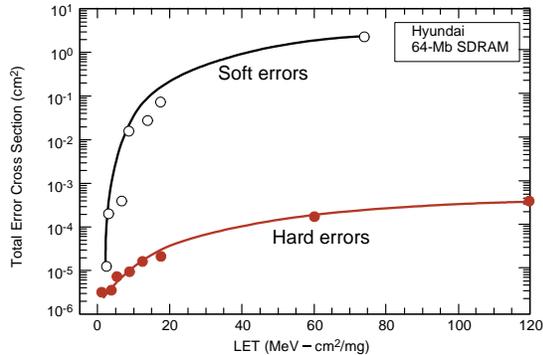

Figure 11. Upset and hard error cross section dependence on LET for an advanced DRAM.

relative number of hard errors is small. However, this can affect EDAC in typical space applications because the stuck bits gradually build up during an extended space mission. Not all DRAMs show such large cross sections for hard errors, but the sensitivity of DRAMs to hard errors has steadily increased with scaling.

B. Microprocessors

Fabrication techniques for microprocessors have advanced more rapidly than for other mainstream semiconductor devices because of the need for extremely high speed in processor applications. Thus, SEU effects in processors provide a good measure of how device scaling affects state-of-the-art devices.

Microprocessor testing is not very straightforward because the devices are so complex, requiring extensive support circuitry (at very high operating frequency) as well as an operating system in order to exercise the device. The operating system is critically important. If it is too complex, then elementary malfunctions of the processor under test will be hidden by malfunctions in the operating system. Recent tests of microprocessors have been based on board-level development systems, designed by the manufacturer, with very simple operating systems. Software can be designed to test device operation at various levels. For example, register-intensive tests can be used that continually evaluate internal registers to isolate SEU effects in various regions of the device. The cache section of modern processors can also be evaluated separately using software techniques. These methods, along with tests at different clock frequencies to determine the effects of internal transients on upset rates, allow basic comparisons to be made in the SEU sensitivity of different types of processors, although they do not answer the more practical question of how many upsets will actually occur in a real software application. Figure 12 shows an example of register-level tests for floating-point registers in a

Power PC750 microprocessor [21]. In this case there is a significant difference in the cross section for "1 to 0" compared to "0 to 1" transitions. Note that the threshold LET for upsets in the processor is about the same as that of the DRAM in Figure 5, even though the internal design and scaling rules for the microprocessor are quite different.

Although the threshold LET for upset in these processors is very low, the number of upsets that will occur in a high-inclination earth is not that high. Correctable errors will occur roughly once every 24 hours, and uncorrectable errors or "crashes" are predicted every few weeks. (Note however, that the number of correctable errors depends on the specific software that the processor is running). These error rates are low enough to consider these unhardened devices in applications that can tolerate occasional operational malfunctions.
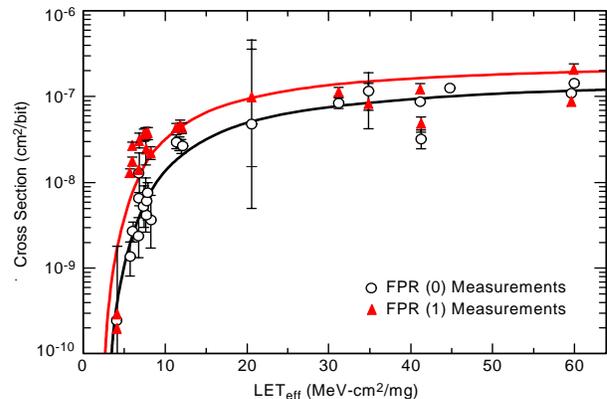

Figure 12. Upset cross section for floating-point registers in the Motorola Power PC750 microprocessor [21].

V. DISCUSSION

A. Upset Sensitivity of Production ICs

The extreme SEU sensitivity that has often been predicted for highly scaled devices has not developed in practice, as can be seen in the earlier results of Figure 4 for DRAMs. Upset in microprocessors involves very different circuitry, without storage capacitors. However, scaling trends for microprocessors also show some reduction in single-event upset sensitivity. Figure 13 compares upset results for three different generations of Power PC microprocessors [22]. The tests were done at maximum frequency, which increased as devices evolved. First note that the upset cross section in the Power PC750 with a feature size of 0.29 μm is slightly greater than the cross section of the G4, with a feature size of 0.2 μm. The core voltage for the two processors are 2.5 and 1.8 V, respectively.
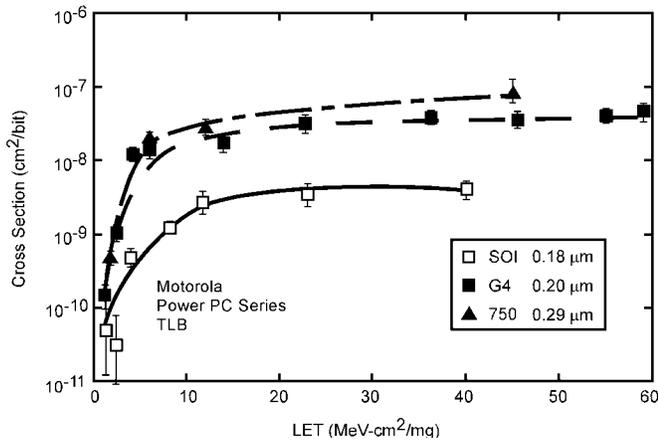
Figure 13. Register error rates for three generations of Power PC microprocessors from Motorola.

Fig. 14. Effect of scaling on saturation cross section for bulk and SOI microprocessors.

Results for the more advanced SOI version of the processor are somewhat different. That device has a feature size of 0.18 µm and core voltage of 1.6 V. The cross section of the SOI device is about an order of magnitude lower than that of the bulk processors, which is expected because the SOI structure has much smaller area than the bulk devices, and cannot collect charge from the substrate. However, the threshold LET is nearly the same as that of the bulk devices, which is inconsistent with earlier scaling projections for SOI devices. This is almost certainly due to excess charge collection because of the parasitic bipolar transistor within the compact SOI MOSFET (the processor is fabricated with partially depleted technology, with a film thickness of about 0.2 µm).

Similar results were obtained for a PowerPC processor that was manufactured by IBM on their SOI process, but used a lower core voltage with a feature size of 0.13 µm. Thus, this SOI result appears to be consistent between two manufacturers. Because the threshold LET is essentially unchanged by scaling, it is possible to compare performance of different microprocessors by means of the saturation cross section. Fig. 14 shows how that parameter changes over several different generations of microprocessors. SOI processors have lower cross sections, which is expected because of the decrease in effective charge collection area for those devices. This result, along with the observation that the LET threshold does not change with scaling, conflicts with the recent modeling results for charge collection shown in Fig. 6. There are many possible reasons, including the difficulty of incorporating the additional highly doped regions shown in Fig. 4 from the more general considerations that are addressed in the semiconductor roadmap.
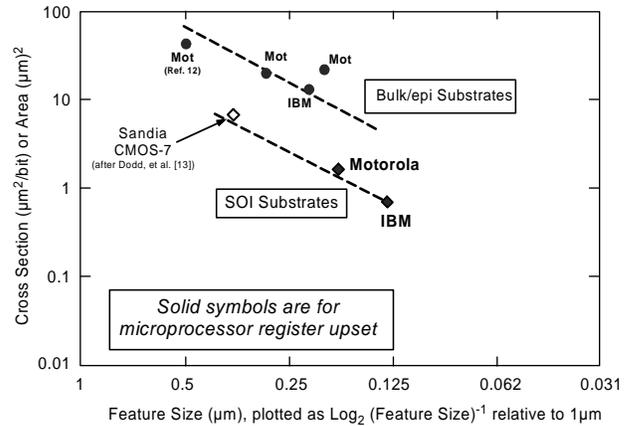
B. Effects of High Frequency on Error Rates

The clock frequency of microprocessors has increased rapidly along with decreased feature size. As the clock frequency increases, the "window" for logic errors from internal transients becomes larger.

Older results for a SPARC processor from a group in France [23] are shown in Fig. 15. These results show a very strong dependence on frequency for a device with a maximum clock frequency of 40 MHz. These results suggest that clock frequency will have a large effect on modern processors, operating at much higher clock frequencies, essentially following the trends that have been assumed by earlier modeling studies regarding frequency dependence and the importance of digital SETs to upset in these devices.
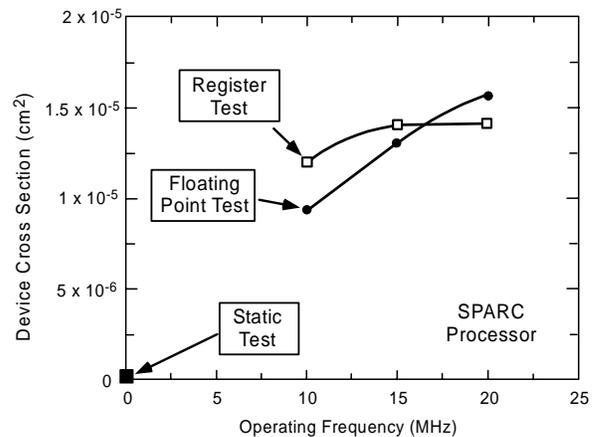

Fig. 15. Frequency dependence of upsets in an older SPARC processor.

However, tests of more advanced devices have not shown such strong frequency effects. Test of PowerPC processors with clock frequencies of several hundred MHz showed no consistent frequency effects when tests at 1/5 to ½ maximum clock frequency were compared.

Recent test results for more advanced SOI processors are shown in Fig. 16, indicating that the cross section increases approximately a factor of two at maximum clock frequency [24], even for devices that operate at clock frequencies of 1-GHz.. This is a very small effect compared to the older results, showing that digital SETs have very little effect, even for advanced devices with very high clock speed.
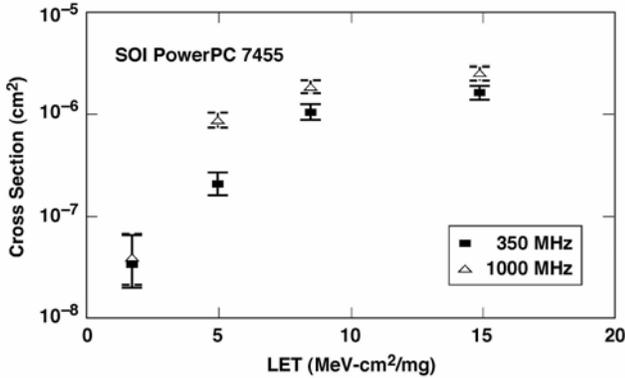

Fig. 16. Effect of clock frequency on SEU cross section for a PowerPC with a maximum clock frequency of 100 MHz [24].

These results, which represent a real, production circuit with feature size of 0.18 µm and 1.6 V core voltage, differ from recent modeling work on test structures that have predicted large increases in SEU rates for devices with such small feature size from transients [25,26]. There are several possible reasons for this, but the most likely is that the internal circuitry used in high-performance microprocessors is designed with larger performance margins than assumed in the modeling work. A complex commercial device must incorporate additional margin so that on-chip distributions in threshold voltage due to statistical variations in the number of dopant atoms do not adversely affect yield. It is quite possible that larger differences in performance would be observed at the circuit level if the processors were operated at higher clock frequencies than they are guaranteed to meet. Nevertheless , these results for high-performance production circuits clearly show far less dependence on clock frequency than expected – or predicted – by modeling studies, even at 1 GHz clock frequency. Although digital SETs may ultimately become the limiting factor for SEU effects in highly scaled devices, that is clearly not the case for mainstream devices at the 0.13 µm technology node, and power supply voltage of 1.1 to 1.3 V.

C. Charge Collection and Soft Error Studies

Charge collection in SOI transistors is very complicated, and is heavily influenced by specific processing techniques. Figure 17 shows how the parasitic transistor gain affects measured error rates using an alpha emitter [27] (this is a standard test that is used by semiconductor manufacturers). All of the devices were made with the same feature size, but special ion implant steps were used for the second SOI process in order to reduce the bipolar transistor gain. The error rate is clearly much lower for the device with lower

gain. Note that without the special implant, the error rate of the SOI device is significantly higher than an equivalent device, fabricated on bulk technology.
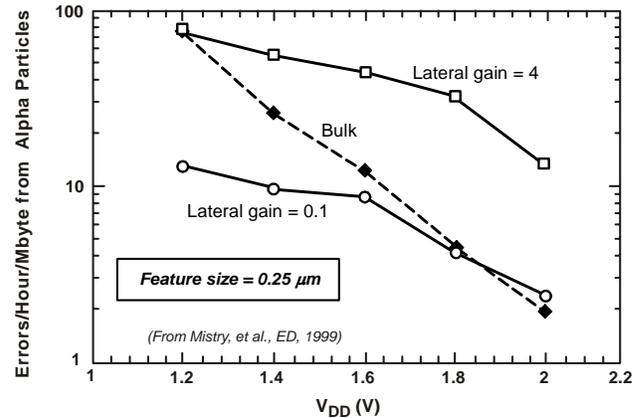

Figure 17 Effect of parasitic bipolar transistor gain on alpha-particle induced upset rates for SOI circuits [27].

In addition to alpha particle upset effects, semiconductor manufacturers are also concerned with upset effects from neutrons at ground level. Figure 18 shows an example of test data for SOI structures from an advanced process that were tested at the Los Alamos neutron facility [28]. They show the expected dependence on collection volume, and also illustrate good agreement between special modeling done by the manufacturer with test data. A great deal of work is being done on atmospheric neutron upset effects by the device community, which can be used to bound upset
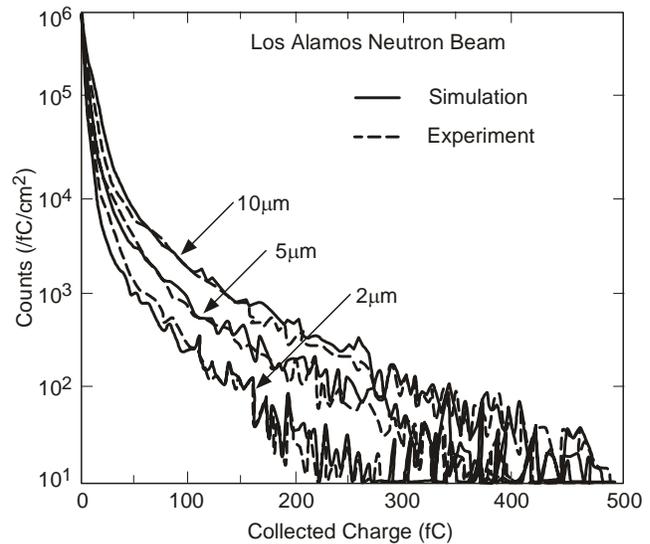
After Tosaka, et al., IEEE Trans. Nucl. Sci., June, 1999

rates in the space environment. However, it is important to

Figure 18 Neutron upset results for commercial memory devices [28].

realize that these commercial products are not hardened in the conventional sense, and will be subject to significant numbers of upsets in space.

Another example of the concern of mainstream manufacturers about neutron soft errors is shown in Fig. 19 after a paper by a group from Intel Corporation [29]. The data in the paper was obtained at the Los Alamos WNR neutron source on 16-Mb SRAMs that are used as test vehicles to evaluate basic performance of different generations.

The paper also discusses SOI processes, but the data in the figure is for bulk CMOS. Their results are normalized to various target power supply voltages, which change with scaling. They predict a slight improvement in soft error rate with scaling, in general agreement with the results obtained by JPL for heavy-ion tests of the PowerPC microprocessors family.
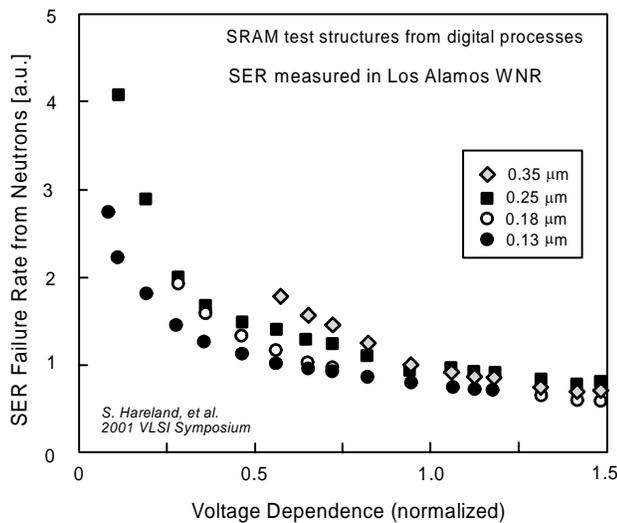

Fig. 19 Normalized neutron soft error rate for several technology generations, using SRAM test structures. Data were taken at the Los Alamos WNR facility.

VI. CONCLUSIONS

This report has discussed some basic concepts and recent trends for single-event upset in highly scaled devices. Most of the results were obtained during the last two years, some from specific radiation tests and others from modeling studies. The results show that the radiation susceptibility has actually improved somewhat for devices that have advanced to the 0.13µm level, which contradicts earlier predictions. This trend is encouraging, but it may not necessarily continue for devices that are scaled below 0.1 µm. It is important to note that the recent computer modeling calculations for SEE susceptibility of scaled devices predicts a large increase in collected charge that is directly in conflict with test results for heavy ions and neutron soft errors. This illustrates the difficulty of making accurate assessments of scaling effects. Note however that the structures used for modeling were not from mainstream manufacturers. The

special techniques used to improve efficiency and confine carriers to narrow regions, such as halo doping, will also affect charge collection in devices with small areas. Additional work needs to be done that includes more representative structures to see if the discrepancy between modeling and experiment can be explained by geometrical differences. Predictions of the importance of digital SETs to upset rates in high-frequency logic devices are clearly at odds with recent data on highly scaled microprocessors, which are the most aggressively scaled devices presently available. The Semiconductor Roadmap has been revised, showing a relatively flat trend for power supply voltage with scaling that is quite different from earlier versions. This will maintain internal noise immunity at levels near that of present technology devices, and may delay the point where digital SETs become important for mainstream technology.

Test data show that the cross section of partially depleted SOI technologies is substantially lower than for bulk technologies with the same feature size, but the threshold LET is nearly the same. The threshold LET results may be coincidental, but have been observed for devices from two different manufacturers with feature sizes of 0.18 and 0.13 µm. The reduced saturation cross section is consistent with the smaller effect area for charge collection in the region of SOI transistors where bipolar amplification is possible.

If fully depleted SOI circuits become available, there may be significant improvement in threshold LET as well as in cross section that will be a major advantage for space applications. However, fully depleted devices will likely be produced on processes with even lower voltages and critical charge, and it is difficult to assess the net effect on SEE susceptibility.

Bulk devices will continue to be scaled to smaller dimensions as well, as shown in the 50 nm transistor structure proposed by the IBM group for mainstream applications in 2007. The scaling trends that have continued from the 500 nm through the 130 nm nodes strongly suggest that scaling will actually improve SEE susceptibility, at t least through the 90 nm node. Fundamental considerations of switching energy and noise margin suggest that sudden changes in SEU sensitivity are unlikely, and that the relatively flat dependence of SEU effects on scaling is likely to continue. However, circuit architecture and functional errors will likely become more important as devices are scaled to even smaller dimensions, and should receive more emphasis in future scaling studies because of the difficulty of dealing with those effects in complex circuits.

REFERENCES

[1] D. Binder, E. C. Smith and A. B. Holman, "Satellite Anomalies from Cosmic Rays," IEEE Trans. Nucl. Sci, **22**(6), 2675 (1975).

[2] E. L. Petersen, *et al*.,"Calculation of Cosmic Ray Induced Soft Upsets and Scaling," IEEE Trans. Nucl. Sci., (**29**)6, 2055 (1982).

[3] S. E. Diehl, *et al*., Error Analysis and Prevention of Cosmic-Ion Induced Soft Errors in Static CMOS RAMs," IEEE Trans. Nucl. Sci., **29**(6), 2032 (1982).

[4] T. C. May and M. H. Woods, "Alpha-Particle Induced Soft Errors in Dynamic Memories," IEEE Trans. Elect. Dev., **26**, **1** (1979).

[5   SIA Industry Roadmap. 2003.

[6] B. Davari, R. H. Dennard and G. G. Shahidi, "CMOS Scaling for High-Performance and Low Power – The Next Ten Years," Proceedings of the IEEE, **89**, 595 (1995).

[7] Y. Taur, *et al*., "CMOS Scaling into the Nanometer Region," Proceedings of the IEEE, **85**, 486 (1997.

[8] D. J. Frank*, et al*., "Device Scaling Limits of Si MOSFETs and Their Application Dependencies," Proc. IEEE, **89**(3), pp. 259-288 (2001).

[9] R. H. Dennard, *et al*., "Design of Ion-Implanted MOSFET's with Very Small Dimensions," IEEE J. Solid State. Circuits, **9**, 256 (1974).

[10] K. Itoh, K. Sasaki and Y. Nakagome "Trends in Low-Power RAM Circuit Technologies," Proc. of the IEEE, **83**(4), pp.524—543 (1995).

[11] K. Takeuchi, R. Koh and T. Mogami, "A Study of the Threshold Voltage Variation for Ultra-Small Bulk and SOI CMOS," IEEE Trans. Elect. Dev., **48**(9), pp. 1995-2000 (2001).

[12] T. Hamamoto, S. Sugiura and S. Sawada, "On the Retention Time Distribution of Dynamic Random Access Memory," IEEE Trans. Elect. Dev., **45**(6), pp. 1300-1309 (1998).

[13] O. Musseau, et al., "Charge Collection in Submicron MOS/SOI Technology," IEEE Trans. Nucl. Sci., **44**(6), 2124 (1997).

[14] P. E. Dodd, "Device Simulation of Charge Collection and Single-Event Upset," IEEE Trans. Nucl. Sci., **43**(2), 561 (1996).

[15] C. M. Hsieh, *et al*., "A Field Funneling Effect on the Collection of Charge from Alpha Particle Tracks in Silicon," IEEE Elect. Dev. Lett., **2**(4), 103 (1981).

[16] F. B. McLean and T. R. Oldham, "Charge Funneling in n- and p-Type Substrates, " IEEE Trans. Nucl. Sci., (**29**)6, 2018 (1982).

[17] H. Shin, "Modeling of Alpha Particle Soft Error Rate in DRAM," IEEE Trans. Elect. Dev.,**46**(19), 1850 (1999).

[18] V. Ferlet-Cavrois, et al., "Charge Enhancement in NMOS Bulk Transistors Induced by Heavy Ion Irradiation," ," IEEE Trans. Nucl. Sci., **51**(6), pp. 3255-3262 (2004).

[19] H. B. Garrett, *et al*., "Single-Event Upset Effects on the Clementine Solid-State Data Recorder," J. Spacecraft and Rockets, **32**(6), pp. 1071-1076 (1995).

[20] L. D. Edmonds, *et al*., "Ion-Induced Stuck Bits in 1T/1C SDRAM Cells," IEEE Trans. Nucl. Sci. **48**(6), pp. 1925-1930 (2001).

[21] G. W. Swift, *et al*., "Single-Event Upset in the Power PC750 Microprocessor," IEEE Trans. Nucl. Sci. **48**(6), pp. 1822-1827 (2001).

[22] F. Irom, *et al*., "Single-Event Upset in Commercial Silicon-on-Insulator PowerPC Microprocessors," IEEE Trans. Nucl. Sci., Dec., 2002.

[23] N. Renaud, "ATMEL TSC695F Radiation Hardened 32-bit Sparc Processor," presented at the 2002 RADECS Workshop, EPadova, Italy, Sept. 2002.

[24] F. Irom and F. Farmanesh, "Frequency Dependence of Single-Event Upset in Advanced Commercial PowerPC Microprocessors," ," IEEE Trans. Nucl. Sci., **51**(6), pp. 3505-3509 (2004).

[25] P. E. Dodd, et al., "Production and Propagation of Single-Event Transients in High-Speed Digital Logic ICs," IEEE Trans. Nucl. Sci., **51**(6), pp. 3278-3284 (2004).

[26] M. Gadlage, et al., "Single Event Transient Pulse Widths in Digital Microcircuits," IEEE Trans. Nucl. Sci., **51**(6), pp. 3285-3290 (2004).

[27] K. R. Mistry *et al*., "Parasitic Gain Reduction and the Optimization of 0.25 um Partially Depleted SOI MOSFETs," IEEE Trans. Elect. Dev., 46(11), 2201 (1999).

[28] Y. Tosaka, *et al*., "Simulation Technologies for Cosmic Ray Neutron-Induced Soft-Errors: Models and Simulation Systems," IEEE Trans. Nucl. Sci., **46**(3), 774 (1999).

[29] S. Hareland, *et al*., "Impact of CMOS Process Scaling and SOI on the Soft Error Rates of Logic Processes," Digest of Papers from the 2001 Symposium on VLSI Technology, pp. 73-74.